REMARKS

After the present amendment, claims 1-6 and 8-46 remain pending in the present application. Claims 1, 5, 13-15, 21-22, 26, 41, 44, and 46 have been amended. Claim 7 has been canceled. Claims 33-40 have been allowed. Reconsideration and allowance of outstanding claims 1-6, 8-32, and 41-46 in view of the above amendments and following remarks are requested.

A. Objection to Claim 5

The Examiner has objected to claim 5, stating that the claim exhibits an informality. Applicants have amended claim 5 as shown above. Consequently, Applicants respectfully request that the objection to claim 5 be withdrawn.

B. Rejection of Claims 1-2, 4-32, and 41-46 Under 35 USC §102(e)

The Examiner has rejected claims 1-2, 4-32, and 41-46 under 35 USC §102(e) as being anticipated by U.S. Patent Application Number 6,597,394 to Duncan, et al. ("Duncan"). For the reasons discussed below, Applicants respectfully submit that amended independent claims 1, 13-15, 21-22, 26, 41, 44, and 46 are patentably distinguishable over Duncan.

As explained in the present application, the time to acquire, process, and compress image data can cause an unacceptable delay when acquiring consecutive images. The delay can last several seconds. This delay is a problem for photographers who need a continuous shooting capability to photograph a sequence of images in quick succession. The present invention solves these and other problems.

In accordance with one embodiment disclosed in the present application in at page 25, line 18 to page 26, line 7:

> "As shown in the example of FIG. 7B, for video processing or other real-time data stream, the buffers of level zero and level one are alternately used for fetching input image data, while the buffers of level two and level three are alternately used for storing output image data. In this way, image data is input, processed and output in every cycle.
>
> The local buffers reduce the address range of the SIMD master controller 450, reduce power consumption by minimizing the number of external memory accesses, and increase the efficiency by allowing long 'burst' data transfers with the external memory. This topology also improves the overall image processing performance without the cost of a complex caching scheme by allowing data fetches and stores to occur in parallel with image processing."

Programmable arithmetic processing block 420 of the present application, shown in Figure 4, is shown in greater detail in Figure 6. Referring to Figure 6 of the present application, in one embodiment, local buffers 500 of levels zero, one, two, and three are shown as part of programmable arithmetic processing block 420.

To clarify the invention, Applicant has amended independent claims 1, 13-15, 21-22, 26, 41, 44, and 46 to recite a programmable arithmetic processor that comprises a first set of local buffers and a second set of local buffers, each buffer in the first set of local buffers alternately used for fetching input image data and each buffer in the second set of local buffers alternately used for storing output image data.

In contrast, Duncan discloses a different programmable image transform processor having programmable addressing and arithmetic blocks. Duncan does not teach, disclose, or suggest a programmable arithmetic processor that comprises a first set of local buffers and a second set of local buffers, each buffer in the first set of local buffers alternately used for fetching input image

data and each buffer in the second set of local buffers alternately used for storing output image data.

Therefore, Duncan does not teach, disclose, or suggest the present invention as defined by amended independent claims 1, 13-15, 21-22, 26, 41, 44, and 46, nor does Duncan achieve some of the advantages of the present invention discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention as defined by amended independent claims 1, 13-15, 21-22, 26, 41, 44, and 46 is not taught, disclosed or suggested by Duncan. Thus, amended independent claims 1, 13-15, 21-22, 26, 41, 44, and 46 are patentably distinguishable over Duncan. As such, the claims depending from the amended independent claims of Duncan are, *a fortiori*, also patentably distinguishable over Duncan for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Rejection of Claims 1 and 3 under 35 USC §102(e)

The Examiner has rejected claims 1 and 3 under 35 USC §102(e) as being anticipated by U.S. Patent Application Number 5,812,195 to Zhang ("Zhang"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Zhang.

In contrast to the present invention, Zhang discloses a system and method for video compression using iterative correction data coding. Zhang does not teach, disclose, or suggest the elements of amended independent claims 1. For example, Zhang does not teach, disclose, or suggest a programmable arithmetic processor that comprises a first set of local buffers and a second set of local buffers, each buffer in the first set of local buffers alternately used for fetching

input image data and each buffer in the second set of local buffers alternately used for storing output image data.

Therefore, Zhang does not teach, disclose or suggest the present invention as defined by amended independent claim 1, nor does Zhang achieve some of the advantages of the present invention discussed above.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by amended independent claim 1 is not taught, disclosed, or suggested by Zhang. Thus, amended independent claim 1 is patentably distinguishable over Zhang. As such, claim 3 depending from amended independent claim 1 is, *a fortiori*, also patentably distinguishable over Zhang for at least the reasons presented above and also for additional limitations contained in dependent claim 3.

D. Rejection of Claim 3 under 35 USC §103(a)

The Examiner has rejected claim 3 under 35 USC §103(a) as being obvious with respect to Duncan in view of U.S. Patent Number 6,100,928 to Hata ("Hata"). Applicants respectfully submit that claim 3 depends from amended independent claim 1, and thus, claim 3 should be allowed at least for the same reasons discussed above in conjunction with patentability of amended independent claim 1.

E. **Conclusion**

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 13-15, 21-22, 26, 41, 44, and 46, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-6, 8-32, and 41-46 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-6, 8-32, and 41-46 and an early Notice of Allowance directed to all outstanding claims 1-6 and 8-46 remaining in the present application are respectfully requested.

Respectfully Submitted,
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